

Report No. FAA-RD-80-38

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AIR TRAFFIC CONTROL FACILITY HARDWARE INTERFACES FOR DISCRETE ADDRESS BEACON SYSTEM



April 1980

Final Report

Document is available to the U.S. public through the National Technical Information Service, Springfield, Virginia 22161.

Prepared for

U.S. DEPARTMENT OF TRANSPORTATION
FEDERAL AVIATION ADMINISTRATION
Systems Research & Development Service
Washington, D.C. 20590

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TABLE OF CONTENTS

SECTI	ON	PAGE
ı.	Introduction	1
II.	En Route Facility Interfaces	2
	2.1 Surveillance Interface	2
	2.2 Communications Interface	4
III.	Terminal ATC Facility Interfaces	9
	3.1 Surveillance Interface	9
	3.2 Communications Interface	12
REFER	ENCES:	13

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SECTION I INTRODUCTION

The Discrete Address Beacon System (DABS), when deployed within the National Airspace System (NAS), will provide surveillance of aircraft equipped with either ATCRBS or DABS transponders. For those aircraft equipped with DABS transponders, a high capacity, ground-air-ground digital communications link is also provided.

Surveillance data and data link services will be provided to Air Traffic Control (ATC) facilities (Terminal and En route). Each DABS sensor will have two digital links to each ATC facility: a two-way communications link and a one-way surveillance link from sensor to ATC.

The purpose of this document is to describe the Terminal and Fn route ATC facility hardware configuration for interfacing with DABS.

SECTION II

EN ROUTE ATC FACILITY INTERFACES

The interconnection between DABS and the En Route Air Traffic Control (ATC) facility is via two completely separate narrow band telephone data links: surveillance and communications, as shown in Figure 2-1.

A one-way surveillance link from the DABS sensor to the en route ATC automation system provides unsmoothed aircraft position reports, one report-per-aircraft-per-scan. Surveillance data formats are specified in Reference 1.

A two-way communications link between the DABS sensor and the en route ATC automation system supports both the data link function between ATC and DABS-equipped aircraft and the control and monitoring of the DABS sensor. This communications link is operated in conformance with the formats and procedures of the Common ICAO* Data Interchange Network (CIDIN) specified in Reference 1. A Front End Processor (FEP) located within the en route facility performs a translation between the CIDIN protocol and the protocol used by the en route 9020 central computer complex (CCC). The FEP/9020 CCC protocol is specified in Reference 2.

2.1 SURVEILLANCE INTERFACE

The surveillance data interface is a unidirectional (simplex) interface which is used for the transfer of surveillance data from the DABS sensor to the en route ATC facility. This interface uses unconditioned type 3002 telephone circuits with a 4800 bit per second (bps) modem for each surveillance channel. Additional channels may be used as necessary to support the data rate at a particular site. When multiple channels are used, each channel operates independently.

The surveillance link modems located at the en route ATC facility are connected to the inputs of the Data Receiving Equipment (DRE). Each surveillance channel modem is connected to a separate DRE channel. The electrical signal characteristics of the interface between the modem and the DRE shall conform to MIL-STD-188C, as defined in FCC Tariff 260.

The surveillance data is preprocessed by the DRE and then input into the 9020 Central Computer Complex (CCC) through a 9020 Common Digitizer (CD) adapter. A separate CD adapter is used for each surveillance channel

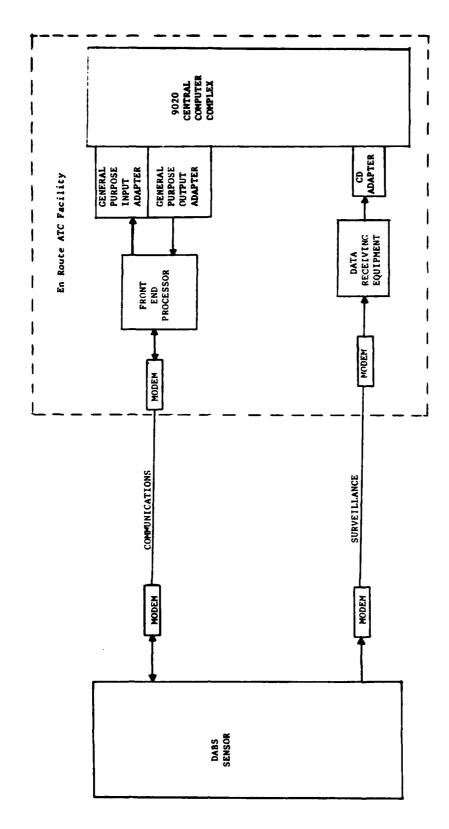


Figure 2-1. DABS/En Route ATC Facility Interfaces

2.2 COMMUNICATION INTERFACE

The communication data interface is a bidirectional, full duplex, interface used for the transfer of status, control and operational ATC messages between the DABS sensor and the en route ATC facility. This interface uses unconditioned type 3002 telephone circuits with 4800 bps modems for each communications channel. The communication data interface modems located at the en route ATC facility are connected to the Front End Processor (FEP). The FEP provides a separate full duplex interface for each DABS sensor communication channel. The electrical signal characteristics of the interface between the modem and the FEP shall conform to MIL-STD-188C as defined in FCC Tariff 260.

The interface between the FEP and the 9020 Central Computer Complex (CCC) is a single bidirectional interface. This interface uses a General Purpose Input (GPI) adapter for transfer of data from the FFP to the 9020 CCC and a General Purpose Output (GPO) adapter for the transfer of data from the 9020 CCC to the FEP.

2.2.1 GENERAL PURPOSE INPUT ADAPTER INTERFACE

The GPI adapter provides an 8-bit plus odd parity parallel interface for transfer of data from the FEP to the 9020 CCC. The signal lines for the GPI interface are as follows:

	ata	a Li	nes		Initiated
Data	In	bit	pos.	P	FEP
Data	In	bit	pos.	0	FEP
Data					FFP
Data	In	bit	pos.	2	FEP
Data	In	bit	pos.	3	FEP
Data	In	bit	pos.	Ą	FEP
Data					FEP
			pos.		FEP
			pos.		FEP

Control Lines	Initiated By
I/O Request In	FEP
Adapter Response Out	Adapter
Device Control Line 1 Out	Adapter
Device Control Line 3 Out	Adapter
Device Control Line 4 Out	Adapter
End of Message (EOM) In	FEP

SIGNAL LINES DESCRIPTION

Data In Lines (Bits 0-7)

The signal levels on these eight parallel lines will be presented to the adapter by the FEP and will be static when the I/O request is detected by the adapter.

Parity Line

The signal level on this line is originated by the FEP to establish odd parity for the associated data lines. The signal will be presented to the adapter and will be static when the I/O request is detected by the adapter.

I/O Request In

The signal level on this line is initiated by the FEP. When an active I/O request signal is detected by the adapter at a time that the adapter is selected and the adapter data register is empty, the adapter will sample the status of the data and parity lines into the adapter data register. The I/O request signal will also be used to sample the EOM line.

By controlling the frequency of the I/O request line, the FEP sets the data transfer rate within system limitation. The FEP will only make the I/O request signal inactive when the adapter response signal is detected by the FEP. The I/O request signal must be made inactive and then active again before the transmission of either another data character or the EOM signal is possible.

Adapter Response Out

An active signal on this line is initiated by the adapter and indicates to the FEP that the adapter has sampled the data, parity, and EOM lines. The Adapter Response Signal will go inactive when the FEP causes the I/O Request Signal to go inactive. The active to inactive transition of the Adapter Response Signal could occur before the associated I/O Request Signal, when inactive, if the channel recognized the termination sequence before the FEP dropped the I/O Request Signal.

Device Control Line 1 Out, Device Control Line 3 Out, Device Control Line 4 Out

The signals of these three lines will be initiated by the adapter when selected to perform a read operation. These signals will remain active until termination of the read operation.

Device Control Line 1 Out

This signal will be up when modifier bit 1 of a read command is set to a "one".

Device Control Line 3 Out

This signal will be up when modifier bit 3 of a read command is set to a "one".

Device Control Line 4 Out

This signal will be up when modifier bit 4 of a read command is set to a "one".

EOM In

Company of the Compan

A signal level on this line is initiated by the FEP and presented to the adapter after the transfer of the last byte of the message has been effected, i.e., the I/O Request and Adapter Response Signals transferring the last byte of the message have been brought inactive. The signal on this line should be presented and static when the I/O Request Signal is detected by the adapter.

Electrical Characteristics

The signal line voltage of +3.7 volts will be used for the active state (one bit) and ground for the inactive state (zero bit).

A detailed description of the operation of the GPI adapter and its interface can be found in Reference 3.

2.2.2 GENERAL PURPOSE OUTPUT ADAPTER INTERFACE

The General Purpose Output (GPO) adapter provides an 8-bit plus odd parity parallel interface for transfer of data from the 9020 CCC to the FEP. The signal lines for the GPO interface are as follows:

Data Lines		Initiated By
Data Out bit pos.		Adapter
Data Out bit pos.	0	Adapter
Data Out bit pos.	1	Adapter
Data Out bit pos.	2	Adapter
Data Out bit pos.		Adapter
Data Out bit pos.	4	Adapter
Data Out bit pos.		Adapter
Data Out bit pos.		Adapter
Data Out bit pos.		Adapter

Control Lines	Initiated By
I/O Request In	FEP
Adapter Response Out	Adapter
Device Inoperative In	FEP
Device Status Line 3 In	FEP
Device Status Line 5 In	FEP
Device Status Line 6 In	FEP
Device Status Line 7 In	FEP
Adapter Selected Out	Adapter
Adapter End of Message (EOM) Out	Adapter

SIGNAL LINE DESCRIPTION

Data Out Line (Bits 0-7)

The signals on these parallel lines will be presented by the adapter to the FEP and will be static when the Adapter Response Signal is detected by the FEP.

Parity Line

The adapter originates a signal on this line to establish odd parity to the associated data lines. This signal level will be presented to the FEP and will be static when the Adapter Response Signal is detected by the FEP.

I/O Request In

The signal level on this line is initiated by the FEP. When the I/O Request Signal is detected by the adapter, and the adapter has a data byte or FOM Out signal to transfer to the FEP, the adapter will initiate an Adapter Response Signal to the FEP. When the I/O Request Signal goes inactive, the adapter will initiate the transfer of the next data byte from the 9020 CCC to the adapter data register. By controlling the frequency of the signals on the I/O Request Line, the FEP sets the data transfer rate within system limitation. The device must assure that signals on device status lines 3,5,6, or 7 are static for sampling when the fall of I/O Request is detected by the adapter.

Adapter Response Out

An active signal on this line is initiated by the adapter when the adapter has a data byte or EOM Out to transfer to the FEP and the I/O Request Signal is active. The Adapter Response Signal will go inactive after the FEP causes the I/O Request Signal to go inactive and the adapter has read the device status lines.

Device Inoperative In

This line is monitored by the adapter whenever the adapter is selected. Upon detection of an active signal (open or ground level) the adapter will also sense Device Status Lines 3,5,6, and 7. Upon detection of a "Device Inoperative" condition, the operation will be terminated and Unit Check presented with Channel End and Device End status.

Device Status Lines 3,5,6, and 7

These lines are monitored by the adapter whenever the Device Inoperative Line is active (ground level or open) or, in the absence of an active Device Inoperative signal, between the fall of I/O Request In and the fall of Adapter Response Out, during a Write operation. Upon detection of a signal(s) on line 3,5, and 6, the operation is terminated. A signal on Device Status Line 7 will not terminate the operation. The FEP shall reset the Device Status Lines after the adapter signals termination by dropping Adapter Selected Out. This will not reset sense register bits that have been set by Device Status Lines.

Adapter Selected Out

A signal on this line is initiated by the adapter and is active whenever the adapter is selected for message transfer (write mode). This signal, detected by the FEP, indicates that the 9020 CCC has a message to transmit. Under normal conditions this signal is brought inactive during the termination sequence. If the Adapter Selected Signal is brought inactive without the EOM signal having been presented to the FEP, the FEP is able to determine that the adapter has been deselected (write operation terminated) by some abnormal condition. There are several abnormal conditions causing the write operation to be terminated: Bus Out Check, Data Check, Device Inoperative, or an active Device Status in Line 3, 5 or 6, detected by the adapter, a Halt I/O condition initiated by the program, a selective reset is issued by the channel, or a system reset occurs. This abnormal condition detection by the FEP may be used to enable the FEP to set up for a retransmission.

Adapter End of Message (FOM) Out

The adapter response signal, resulting from any active I/O request from the FEP, is used by the FEP to sample the adapter EOM signal (the data lines are not valid when the active adapter EOM signal is sampled). The fall of the I/O Request In that transferred the EOM signal to the FEP will cause the adapter to initiate the termination of the write operation. Use of Adapter FOM is optional. If EOM is not used, Adapter Selected Out going inactive signals the End of Message.

Electrical Characteristics

The signal line voltage of +3.7 volts will be used for the active state (one bit) and ground for the inactive state (zero bit).

A detailed description of the operation of the GPO adapter and its interface can be found in Reference 3.

SECTION III

TERMINAL ATC FACILITY INTERFACES

The interconnection between DABS and the Terminal Air Traffic Control (ATC) system is via two completely separate narrow band telephone data links: surveillance and communications as shown in Figure 3-1.

The surveillance link consists of two separate and independent one-way channels from DABS to the terminal ATC facility. One channel supports the ARTS III data processing subsystem (DPS) and the other channel supports the Video Reconstitutor. Each surveillance channel carries a data stream of radar, beacon, radar reinforced beacon, and weather messages. The only difference between the two channels is that the sensor reformats all DABS transponder reports as ATCRBS reports prior to dissemination to the Video Reconstitutor. This is required to perform conventional beacon decoding of the reconstituted video. Surveillance message formats are specified in Reference 1.

The Video Reconstitutor is an independent, self contained unit located at the ARTS III ATC facility. It provides a parallel path from the telephone line to the display by converting the narrow band digital surveillance messages to rho-theta ATCRBS beacon, radar and weather video formats for use on time-shared displays such as the ARTS III Data Entry and Display Subsystem (DEDS). The Video Reconstitutor also internally generates Azimuth Change Pulses (ACP), Azimuth Reference Pulse (ARP), radar and beacon pretriggers such that a broad band link between transmitter and indicator site is not required for its proper operation. In the event of an ARTS III DPS failure, the Video Reconstitutor continues to operate, providing video aircraft positional and weather information to the DEDS.

The communications link between the DABS sensor and the ARTS III facility is a two-way link which supports both the data link function between ATC and DABS-equipped aircraft and the control and monitoring of the DABS sensor. Transmission of communications messages on this link is in conformance with CIDIN protocol and the message formats specified in Reference 1.

3.1 SURVEILLANCE INTERFACE

The surveillance data interface is a unidirectional (simplex) interface used for the transfer of surveillance messages from the DABS sensor to the terminal ATC facility. This interface uses unconditioned type 3002 telephone circuits with 4800 bps modems for each surveillance channel. Multiple channels will be used to expand the single channel transfer rate of 4800 bps as required to support the data rate at a particular site.

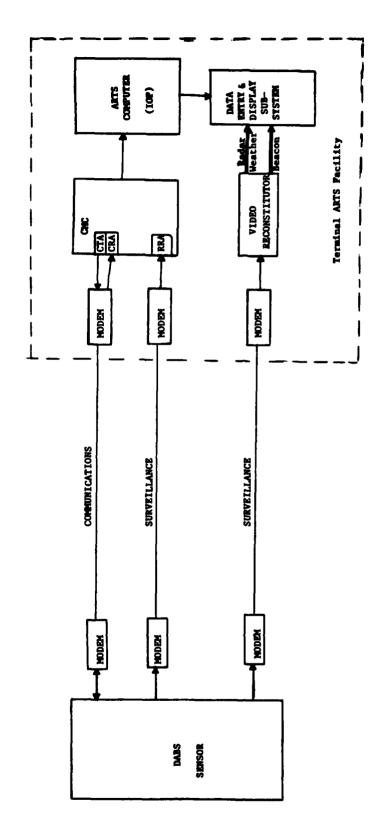


Figure 3-1. DABS/rerminal ATC Facility Interfaces

The surveillance link modems located at the terminal ATC facility are connected to the inputs of the Radar Receiver Adapter (RRA) and the Video Reconstitutor. The electrical signal characteristics for the modem digital interface shall conform to MIL-STD-188C, as defined in FCC Tariff 260.

3.1.1 RADAR RECEIVER ADAPTER

The Radar Receiver Adapter is a part of the Communications Multiplexer Controller (CMC) which converts the narrow band surveillance data for high speed input to the ARTS III DPS. A separate Radar Receiver Adapter is used for each channel.

3.1.2 VIDEO RECONSTITUTOR

A separate, independent surveillance link is interfaced to the Video Reconstitutor. The Video Reconstitutor converts digital surveillance data into analog video signals for presentation on the ARTS Data Entry and Display Subsystem (DEDS) time-shared displays. The characteristics of the data on the interface between the Video Reconstitutor and the DEDS shall be as follows:

1. ACP/ARP

ACP's	4096 per 360 degrees of antenna rotation equally spaced for constant rotation rate.
wlac-to-pulac	+ 10% of normal enacing

ACP pulse-to-pulse	+	10%	of	normal	spacin
jitter					

ARP	jitter	<u>+</u>	20%	ΟÌ	ACP	normal	spacing

Pulse	Amplitude	5	volts	peak-to-peak
1 4100	Imprione	-		France I

2. Beacon Video

Amplitude	2.0 - 4.0 volts
Rise time	.0515 microsecond
Fall time	.125 microsecond

Radar Video

Amplitude	2.0 - 4.0 volts
Rise/fall time	.2 microsecond

4. Radar Pre-triggers

Amplitude 30 - 90 volts

Position 20 to 120 microseconds

before radar range 0

Pulse Width 1 microsecond + 0.5

Rise time less than 20% of pulse

width

A detailed description of the DEDS and its interface can be found in Reference 4.

3.2 COMMUNICATION INTERFACE

The communication data interface is a bidirectional, full duplex, interface used for the transfer of status, control, and operational ATC messages between the DABS sensor and the terminal ATC facility. This interface uses unconditioned type 3002 telephone circuits with 4800 bps modems.

The communications link modem located at the terminal ATC facility will be connected to the ARTS computer complex through a Communications Transmitter Adapter (CTA) and a Communications Receiver Adapter (CRA). These adapters are part of the Communications Multiplexer Controller (CMC). A detailed description of the CMC can be found in Reference 5.

The electrical characteristics of the digital interface to the modem shall conform to MIL-STD-188C, as defined in FCC Tariff 260.

The communications link protocol is the CIDIN protocol specified in Reference 1.

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